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# **Design and Performance of Different Low Power Full Adder Topologies using CMOS Technology**

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**ABSTRACT:** In this project different types of Full Adder are designed using CMOS Technology. To implement Complementary Metal Oxide Semiconductor (CMOS) Logic technology many logic styles are employed, one example is full adder which is the circuit one of the most important digital functional blocks used in arithmetic and logic unit. The proposed full adder topologies present different low power and high-speed full adder designs for digital arithmetic circuits: 6T, 8T and 10T. Each design uses a different number of transistors to implement the full adder, achieving varying level of power consumption and speed. The aim of this project is to design a different full adder design using CMOS with low consumption of power and high performance. The proposed full adders circuits are designed using 0.12 $\mu$ m CMOS technology at 1.2V supply voltage. DSCH is used to validate the architecture of the logic circuit and Microwind tool is used for designing and simulating circuits at layout level.

**KEYWORDS:** CMOS; Full adder; Power consumption; Layout.

## **I. INTRODUCTION**

Binary addition is facilitated by a fundamental digital component known as a full adder. This circuit combines three input bits, producing a sum and a carry-out signal. The full adder plays a critical role in digital arithmetic, enabling computers and other electronic devices to perform calculations. By processing three inputs and generating two outputs, the full adder ensures accurate binary addition, including the transfer of values to subsequent bit positions. This essential function makes the full adder a cornerstone of digital electronics and computing systems.

## **II. FULL ADDER**

In digital electronics, full adders serve as essential building blocks for arithmetic operations. By integrating three binary inputs, these circuits produce a sum and carry-out signal, facilitating precise calculations. The full adder's ability to handle binary addition with carry-over values makes it a crucial component in various digital systems, from simple calculators to complex computing architectures. Its functionality enables efficient and accurate processing of binary data, underpinning many modern technological advancements.

## **III. PROPOSED FULL ADDER DESIGN**

A 10-transistor full adder is a highly optimized design used in low power, high speed digital circuit. The proposed 10T full adder is achieve low power consumption, high speed and reduced transistor count compared to conventional full adders. The proposed circuit is built using 5 NMOS and 5 PMOS transistors. Four transistors for XOR logic and Six transistors for MUX based approach.

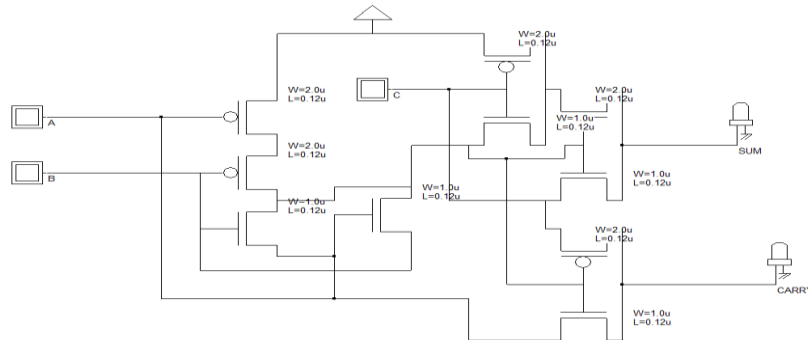


Fig 1 Proposed 10T full adder design

A novel design of 8T full adder designed on the logic of two 3T XOR and one 2T MUX. So in total 8 transistor.

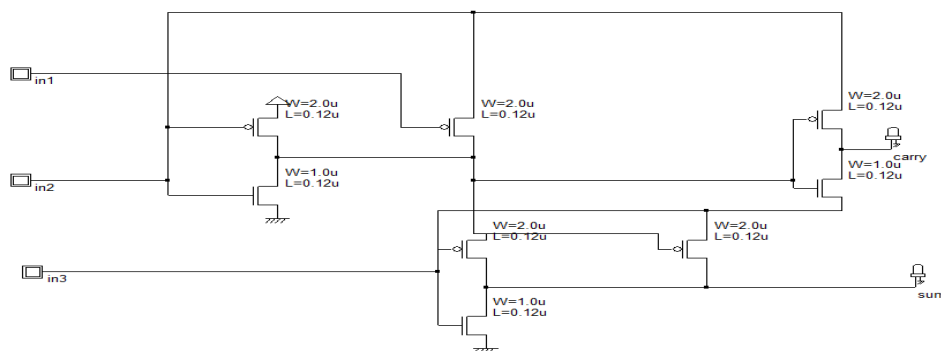


Fig 2 Proposed 8T full adder design

The 6-transistor full adder is an ultra-compact and efficient arithmetic circuit design using PTL. The proposed 6T FA designed using two 2T XOR and one MUX. The proposed full adders achieve better result than 8T, 10T in terms of power, delay and power delay product. The 6T full adder circuit is designed using 0.12μm CMOS technology at 1.2V supply voltage.

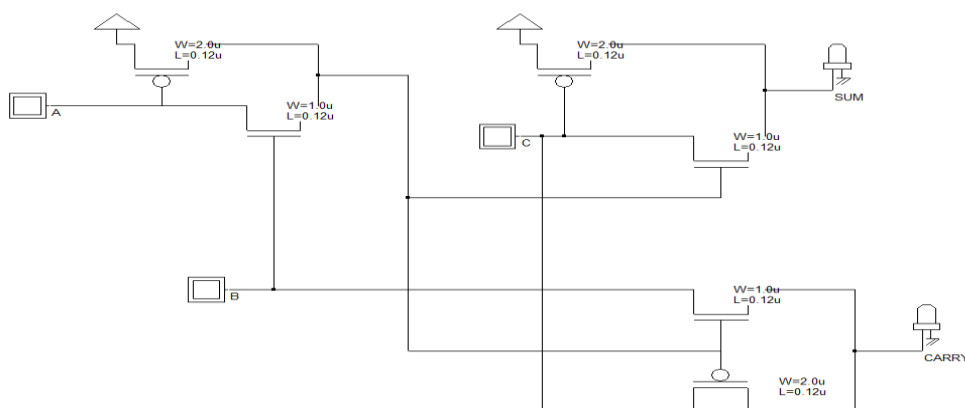


Fig 3 Proposed 6T full adder design



Table 1 Comparison between Full Adder and Proposed Full Adder design

Design	Number Of Transistor	Power (mW)	Delay (ns)	PDP
Full Adder	28	5.55	19.67	109
10T Full Adder	10	0.439	8	3.312
8T Full Adder	8	0.368	3.018	1.11
6T Full Adder	6	0.25	1.95	0.492

#### IV. SIMULATION RESULTS

The proposed full adder with minimum of 8 transistor with high speed and low power consumption, which employs a two 3T XOR and 2T MUX. The proposed 10T circuit is built using 5 NMOS and 5 PMOS transistors. Four transistors for XOR logic and Six transistors for MUX based approach. The proposed full adder schematics are drawn using 0.12 $\mu$ m CMOS technology with 1.2 V supply voltage. Simulation results shows the great improvement in terms of power delay product. The 6T full adder consumes an average power of 0.252mW. The power consumption increases with the number of transistors. The critical path delay of the 6T FA measured at 0.492 ps.

Fig 4 shows Microwind layout of 8T full adder using 0.12 $\mu$ m CMOS technology with 3 input and 2 output.

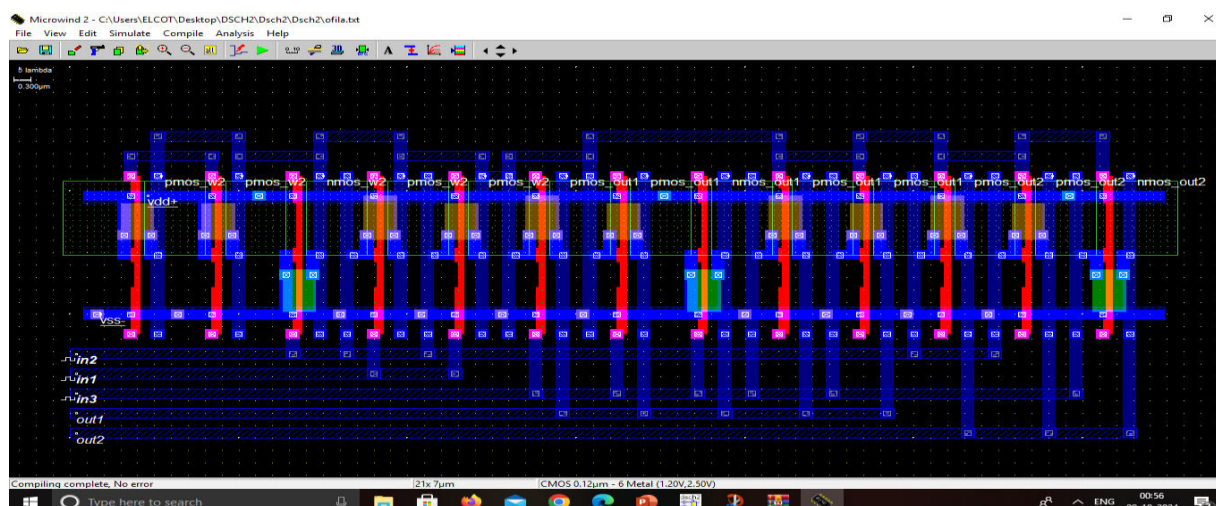


Fig 4 Layout Design of the Proposed Full Adder

The power consumption of a proposed 10T full adder is 0.439 mW. Fig 5 shows simulated output waveform of voltage vs time with 0.439 mW. Delay of the 10T full adder is 8 ns. The power delay product(PDP) of 10T full adder is 3.512 aJ.

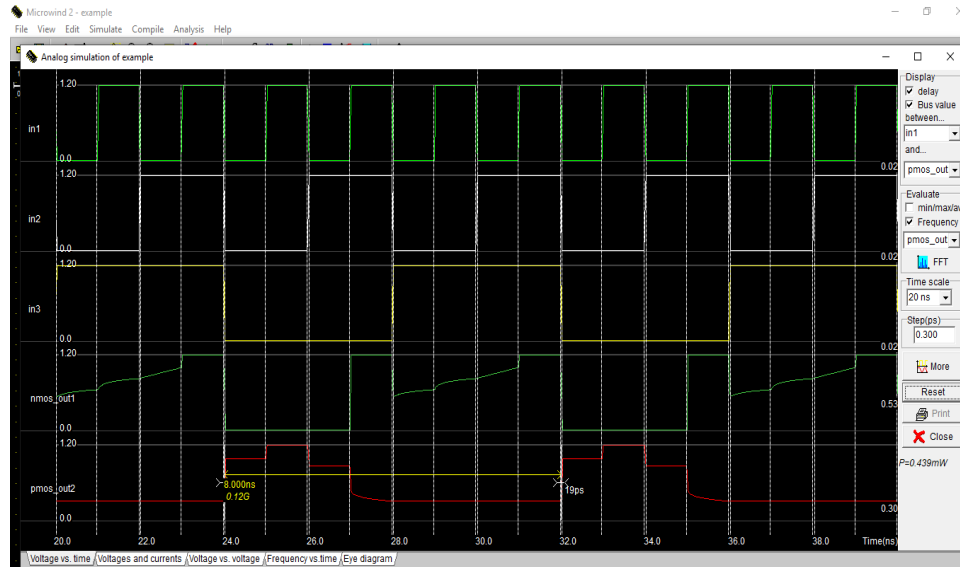


Fig 5 Simulated Output Waveform of 10T Full Adder Design

The power consumption of a proposed 8T full adder is 0.368mW. Fig 6 shows simulated output waveform of voltage vs time with 0.368 mW power. delay of the 8T full adder is 3.018 ns. The power delay product (PDP) of 8T full adder is 1.11aJ.

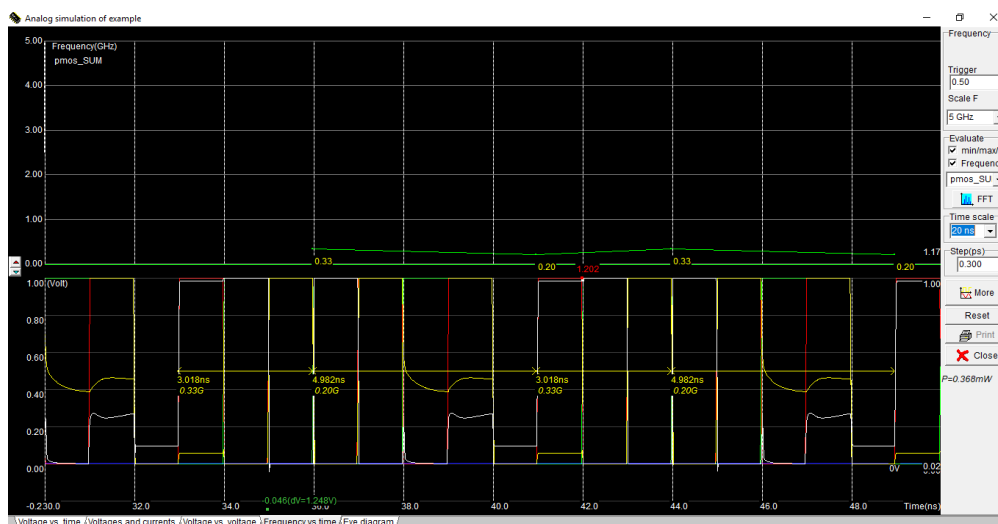


Fig 6 Simulated Output Waveform of 8T

The power consumption of a proposed 6T full adder is 0.252 mW. Delay of the 8T full adder is 1.956ns. The power delay product (PDP) of 6T full adder is 0.492 aJ.

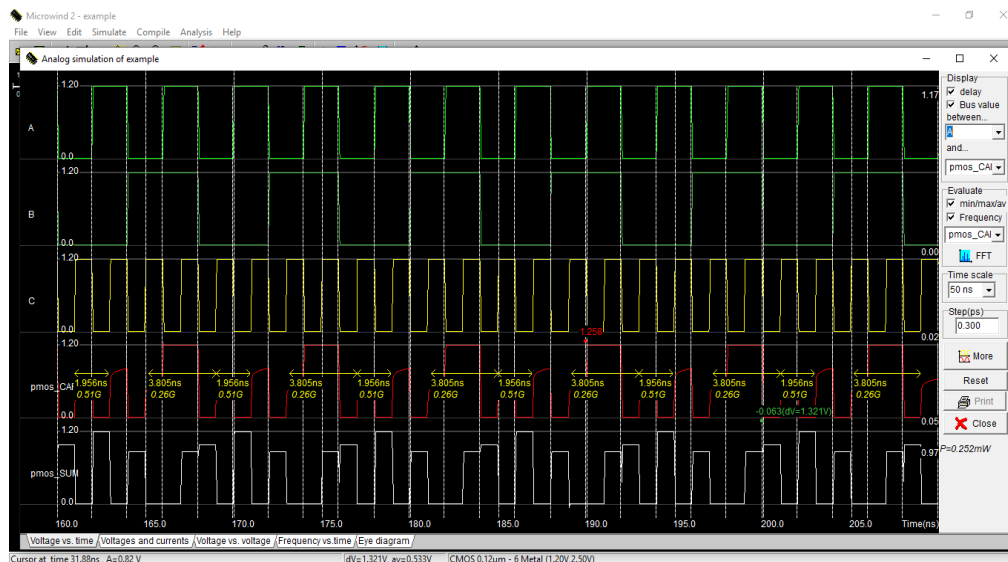


Fig 7 Simulated Output Waveform of 6T

## V. CONCLUSION

In this paper different types of Full Adder are designed using CMOS Technology. A novel design of 8T full adder, which is designed on the logic of two 3T XOR and one 2T MUX. The proposed 10 transistor full adder is designed using 5 PMOS and 5 NMOS CMOS logic style. The 6T FA designed using two 2T XOR and 2T MUX. The Proposed Full Adder is simulated using the DSCH tool and 3D layout of Proposed Full Adder is designed using Microwind tool. The Power supply of the Proposed full adder is 1.2 voltage. The Small number of transistors has higher performance. The power consumption and of the proposed 10T full adder is 0.439mW .The delay of the eight transistor full adder is 8 ns. The power consumption and of the proposed 8T full adder is 0.368 mW .The delay of the eight transistor full adder is 3.018 ns. The 6T Full adders has an improvement for various parameters like power consumption, speed performance and structure size. The power consumption and of the proposed 6T full adder is 0.252 mW .The delay of the six transistor full adder is 1.956 ns. which is lower than the conventional full adder. The proposed 6T full adder gives better calculation of PSD by using 0.12 $\mu$ m CMOS technology. The Power Delay Product of 6 transistor full adder is 0.492. The proposed full adders achieve better result than 8T, 10T in terms of power, delay and power delay product. It is suitable for low energy application and portable devices.

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